REISSUE
Application
for
United States Letters Patent

To all whom it may concern:

Be it known that we,

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have invented certain new and useful improvements in

MEMORY CONFIGURATION OF A COMPOSITE MEMORY DEVICE

of which the following is a full, clear and exact description:

MEMORY CONFIGURATION OF A COMPOSITE MEMORY DEVICE

This is a divisional of application Ser. No. 09/080,696 filed May 18, 1998 now U.S. Pat. No. 6,715,292.

FIELD OF THE INVENTION:

This invention is generally related to a memory device of a whole category of electronic equipment aboard a computerized personal organizer, a handset, a voice recognition device, a voice memory device, and a computer etc. and more particularly related to a composite memory system of a flash memory device.

BACKGROUND OF THE INVENTION

There are many kind of memory devices, for example, mask ROM, erasable programmable read-only memory (EPROM), flash memory and so on. The mask ROM is sintered information data of control command etc in accordance with specifications of users with a production process. Therefore, the mask ROM is unable to rewrite the sintered information data after production. The EPROM is capable of erasing information data by irradiation with ultraviolet lights. However, the EPROM is also unable to electrically erase and rewrite the information data. Therefore, the flash memory device is receiving attention as one of a memory device among the electronic industry. Because of this, the flash memory device is becoming prevalent as an alternative memory device of the mask ROM and the EPROM.

As an electrically erasable memory device, there is an electrically erasable programmable read only memory (EEPROM). Erase operation of the conventional EEPROM is generally based upon one bit unit. On the other hand, erase operation of the flash memory is based upon block unit. Therefore, by the adoption of an erasing by block unit or being one unit of 1 bit, the flash memory device is paid attention as the next generation alternative memory of dynamic random access memory (DRAM) that the integration of the flash memory is far in excess of one of the DRAM market.

Furthermore, the flash memory has obtained a great support from user because of advantages that flash memory is capable of rewriting the data under on board and of being debugged until just before shipment.

Referring to FIG. 1, one of conventional prior arts in a memory system includes a flash memory such a single memory array 2. The memory array 2 has 4 M bits and is divided into plural sector. When the data in the memory element is distinguished under the control of CPU (not shown), the data is sequentially erased with sector unit from the first sector in the memory array 2 or with sector unit from selected sectors.

Address signal A0–A18 are applied an X decoder 6 and an Y decoder 8 with via an address latch 4. The X decoder 6 selects word line in the memory array 2. And also the Y decoder 8 selects bit line in the memory array 2 via an Y gate/sensing amplifier 10.

Programming voltage generator 14 generates a programming voltage for writing data in the memory device 2. Erase voltage generator 16 generates an erase voltage for erasing data in the memory device 2. The programming voltage generator 14 and the erase voltage generator 16 output the programming voltage and the erase voltage into the X decoder 6, the Y decoder 8, and the memory array 2 each other.

An input/output buffer 20 and a data latch 18 are employed for input or output of data. A timer 22 and a system control register 24 are also employed in this system. The system control register 24 input a write enable signal (/WE), an output enable signal (/OE), a chip enable signal (/CE) and voltage supply, Vcc, GND as control signals. The /WE signal is a start signal of the writing operation of the memory array 2. The /OE signal is a start signal of the reading operation of the memory array 2. Further, the /CE signal is a select signal whether the device 1 is selected or the other device is selected.

As for a flash memory, writing operation and erasing operation requires long time in comparison with reading operation. Therefore, a memory device is ideal if the CPU or the other controllers are capable of carrying out the reading operation of the data in the memory array 2 when the other area of the memory array 2 is written or erased under aboard a circuit board.

However, the memory device 1 as shown FIG.1 can not carry out above mentioned parallel processing. .

The 4 M bits capacity's flash memory 2 is formerly used. For example, when the above standard capacity's flash memory 2 is installed as a memory array and the size of software is bigger, the memory array 2 becomes lacking in memory capacity. Therefore, if the large size software is employed, the memory device needs to install a flash memory of the larger capacity. However, it is connected to a cost up to install the memory of the needlessly large capacity.

Thereupon, it is conceivable to employ the plural device as shown FIG. 1 in order to solve the above problem. Still furthermore, in this case, space savings is not able to be materialized, beside a cost goes up by setting up the same plural memory device.

A concurrent flash memory system such as disclosed in a specification of AT29C432 made of ATMEL Company. The contents of this reference being incorporated herein by reference. The above concurrent flash memory employs the two different type memories that are EEPROM and flash memory in a single device. The concurrent flash memory system of the ATMEL is capable of reading the data of the EEPROM while writing operation of the flash memory in one device.

However, the present inventor identified that the system of ATMEL requires the long time erasing the data on the memory device. Because the EEPROM employed by the system of ATMEL is possible only the writing and also erasing with one bit unit. Accordingly, one sector of the flash memory is 8K byte unit and EEPROM of ATMEL unable to store comparatively large data such as a voice data to one sector. The EEPROM requires comparatively long time to erasing operation when the large size data such as voice etc. is stored and located in astride to plural sector of the flash memory.

Furthermore, the present inventor also identified that conventional erasing operation of the data on a memory requires long time in order to erase by the sector unit. The conventional erasing operation is a single sector erasing mode and a plural sector erasing mode. Although the plural sector erasing mode can erase some number of sectors on the flash memory, the selected plural sector is erased to each sector in turn.

Although the flash memory has a batch erasing mode, the batch erasing mode has erased to the data that does not want to erase.

SUMMARY OF THE INVENTION

To solve the above and other problems, according to one aspect of the present invention, A composite flash memory

device includes a plural sector flash memory array which is divided to plural sector that is a minimum erasing unit of the flash memory device, a flash memory array storing control commands which control a total system of the composite flash memory device and/or the only composite flash memory device in and sharing I/O line of the plural sector flash memory array, the read operation of the flash memory array is enable when the plural sector flash memory array is gained access.

According to another aspect of the present invention, a composite flash memory device according to claim 1, further includes a selector selecting an single sector erasing mode which the sectors of the flash memory device are erased by a sector unit and a simultaneously plural sector erasing mode that simultaneously erases the sectors of a regular range in the plural sector flash memory device.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects and further features of the present invention will become apparent from the following detailed description when read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a block diagram of the conventional memory system that has a single memory device according to the prior art;

FIG. 2 is a block diagram of the composite memory device according to the present invention;

FIG. 3 is a structure of the flash memory according to the present invention;

FIG. 4 is a block diagram for the selection whether the single sector erasing mode which a single sector is erased or the plural sector erasing mode which the plural sector are erased of the selector of the composite memory device according to the present invention;

FIG. 5 is a conceptional block diagram of the relation between the control signal block and the data block according to the present invention; and

FIG. 6 is a conceptional block diagram of the relation between the control signal block and the data block which both blocks are located in same memory area according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A description will now be given of preferred embodiments according to the present invention.

Referring now to the drawings, wherein like reference numerals designate corresponding structure throughout the views, and referring in particular to FIG. 2, one preferred embodiment of the composite flash memory device 100 according to the present invention includes two flash memory arrays 12A and 12B which has different number of sector each other. The flash memory array 12A is for storing control programs by which a CPU (not shown) controls the total system. The flash memory array 12A is not divided into plural sector, therefore has single sector of 4M bits.

On the other hand, the flash memory array 12B is for storing data such as image and voice etc and is divided into 2560 sectors, each sector comprised of 128 bytes. Here, the each sector is the minimum unit of the data erasing. The address where was input from the outside is input to an X decoder 8 and also an Y decoder 6 via an address latch 4. As they mentioned above, the X decoder 6 and the Y decoder 8 select the word line and also the data line between the flash memory 12A and the flash memory 12B on the basis of the

input address. An access of the flash memory 12A and 12B is selectable by switching between a program flash enable (/PFE) signal and a data flash enable (/DFE) signal. The /PFE signal enables the access to a flash memory 12A. The /DFE signal enables the access to a flash memory 12B. Y gate/sensing amplifier 10A and 10B is provided to sense and select the bit line in the both flash memories 12A and 12B each other. The Y gate/sensing amplifier 10A and 10B are connected to the same input/output buffer 20 via data latch 18A and 18B each other.

A programming voltage generator 14 supplies program voltages into the X decoder 6, the Y decoder 8 and the flash memories 12A and 12B during programming operation. Similarly, an erase voltage generator 16 supplies erasing voltages into the X decoder 6, the Y decoder 8 and the flash memory 12A and 12B during erasing operation.

In this embodiment, an explanation of the /WE signal and the /OE signal omits because the above signals are same as the above-related art. But, the present embodiment employs the /PFE signal and the /DFE signal such as alternate the chip enable signal (/CE).

An output control circuit 30 generates a ready signal (RY) or a busy signal (BY) and output them to host system (not shown). The RY signal and the BY signal show whether during an automatic algorithm execution or not.

The X decoder 6 and the Y decoder 8 are provided with each flash memory 12A and 12B each other in order to be gotten access to.

When the CPU order the writing operation, the writing algorithm is automatically carried out. When the CPU order the erasing operation, the CPU designates the composite flash memory device 100 whether one sector or certain range of sectors in the flash memory array 12B. The ordered flash memory device 100 automatically carries out the erasing operation on the basis of the erasing mode whether single sector or certain ranges of the sectors in the flash memory array 12B. When plural sector erasing mode is selected, the selected first sector of the ranges is erased at first and then the next sector is sequentially erased until the selected final sector by the automatic erasing algorithm.

The selection between the /DFE signal and the /PFE signal is capable of getting access to the flash memory array 12A which stores the program software during the writing or the erasing operation starts when the data flash memory array 12B is selected by the DFE signal.

Accordingly, the reading access to the data of the flash memory array 12A becomes enable when the data of the flash memory array 12B is erased or written.

Now referring to the FIG. 3, the flash memory array 12B is of the structure which has plural block made up of 64 sectors each, each sector comprises of 128 bytes. Therefore, the one block of the flash memory array 12B is total 8K bytes.

In this embodiment, the composite flash memory device 100 is capable of erasing the only one sector comprised of 128-byte unit, also erasing one block comprised of 8K byte unit (64 sectors) and furthermore, erasing certain range of plural 8K byte unit.

In the case that the composite flash memory device 100 erases the certain range of the sectors, or the block, the selected first sector of the range is erased at first and the next sector is sequentially erased along the sector order.

Now referring to FIG. 4, a selector circuit 39 is located in the composite flash memory device 100 and can select two erasing modes. One mode is a single erasing mode that